

What is claimed is:

1. A vector information processing apparatus comprising:

5 a CPU comprising a plurality of asynchronously operating units;

a main memory for storing data; and

a main memory controller for controlling the writing of data in said main memory, said main memory controller having a VSC address buffer for holding a storage address in said main memory for each element designated by a vector scatter instruction, for inhibiting the outputting of a writing permission signal for said main memory which is generated according to a writing request for writing an element having a smaller element number, which has the same storage address and which has not been processed in a sequence of element numbers, of writing requests for writing elements in said main memory which are issued respectively from said asynchronously operating units according to a vector scatter instruction.

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2. The information processing apparatus according to claim 1, wherein said main memory controller has a plurality of VSC address buffers corresponding respectively to said asynchronously operating units.

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3. The information processing apparatus according to claim 2, wherein said asynchronously operating units impart one identifier to a plurality of said writing requests issued according to a single vector scatter instruction, and said main memory controller clears the contents of said VSC address buffers if an identifier of a preceding writing request and an identifier of a following writing request do not agree with each other.

4. The information processing apparatus according to claim 1, wherein said main memory controller comprises:

a VSC address buffer controller for controlling said VSC address buffer to hold said storage address sent from said asynchronously operating units and, if said VSC address buffer suffers an overflow, requests the asynchronously operating unit which has issued a vector scatter instruction that has caused said overflow to resend said element; and

wherein said asynchronously operating unit has a retry buffer for holding each element designated by said vector scatter instruction issued thereby, and resends an element held by said retry buffer to said main memory controller if requested by said main memory controller to resend said element.

5. The information processing apparatus according to claim 4, wherein said asynchronously operating unit corrects the element number of an element which starts to be resent based on a smallest element number, of the elements which start to be resent by each asynchronously operating unit.

6. The information processing apparatus according to claim 4, wherein if said main memory controller detects a deadlock state in which an overflow of said VSC address buffer and a resending of an element from said asynchronously operating unit are repeated, said main memory controller sends a delay value for shifting the timing to resend the element from said asynchronously operating unit to said asynchronously operating unit; and

wherein said asynchronously operating unit delays the timing to resend the element by said delay value received from said main memory controller.

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7. The information processing apparatus according to claim 5, wherein if said main memory controller detects a deadlock state in which an overflow of said VSC address buffer and a resending of an element from said asynchronously operating unit are repeated, said main memory controller sends a delay value for shifting

the timing to resend the element from said
asynchronously operating unit to said asynchronously
operating unit; and

wherein said asynchronously operating unit
5 delays the timing to resend the element by said delay
value received from said main memory controller.

8. The information processing apparatus according
to claim 4, wherein the number of storage addresses held
10 by said VSC address buffer is set to at least (the
number of elements simultaneously processed by said
asynchronously operating unit) + 1.

9. The information processing apparatus according
15 to claim 5, wherein the number of storage addresses held
by said VSC address buffer is set to at least (the
number of elements simultaneously processed by said
asynchronously operating unit) + 1.

20 10. The information processing apparatus according
to claim 6, wherein the number of storage addresses held
by said VSC address buffer is set to at least (the
number of elements simultaneously processed by said
asynchronously operating unit) + 1.

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11. A method of controlling a memory of a vector information processing apparatus having a CPU comprising a plurality of asynchronously operating units, a main memory for storing data, and a main memory controller
5 for controlling the writing of data in said main memory, said main memory controller having a VSC address buffer for holding a storage address in said main memory for each element designated by a vector scatter instruction, said method comprising the step of:

10 inhibiting the outputting of a writing permission signal for said main memory which is generated according to a writing request for writing an element having a smaller element number, which has the same storage address as said storage address and which
15 has not been processed in a sequence of element numbers, of writing requests for writing elements in said main memory which are issued respectively from said asynchronously operating units according to a vector scatter instruction.

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12. The method of controlling a memory according to claim 11, further comprising the step of:

 holding only storage addresses for a plurality of elements designated by a single vector scatter
25 instruction, in said VSC address buffer.

13. The method of controlling a memory according to claim 11, further comprising the steps of:

imparting one identifier to said writing requests issued according to a single vector scatter instruction; and

clearing the content of said VSC address buffer if an identifier of a preceding writing request and an identifier of a following writing request do not agree with each other.

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14. The method of controlling a memory according to claim 12, further comprising the steps of:

imparting one identifier to said writing requests issued according to a single vector scatter instruction; and

clearing the content of said VSC address buffer if an identifier of a preceding writing request and an identifier of a following writing request do not agree with each other.

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15. The method of controlling a memory according to claim 11, further comprising the steps of:

controlling said VSC address buffer to hold said storage address sent from a plurality of said asynchronously operating units;

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if said VSC address buffer suffers an overflow,
requesting the asynchronously operating unit which has
issued a vector scatter instruction that has caused said
overflow to resend said element; and

5 holding each element designated by said vector
scatter instruction in said asynchronously operating
unit, and resending an element held by a retry buffer to
said main memory controller if requested to resend said
element.

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16. The method of controlling a memory according
to claim 15, further comprising the step of:

 correcting the element number of an element
which starts to be resent based on a smallest element
15 number, of the elements which start to be resent by each
asynchronously operating unit.

17. The method of controlling a memory according
to claim 15, further comprising the step of:

20 if a deadlock state in which an overflow of
said VSC address buffer and a resending of an element
from said asynchronously operating unit are repeated is
detected, sending a delay value for shifting the timing
to resend the element from said asynchronously operating
25 unit from said main memory controller to said
asynchronously operating unit;

wherein said asynchronously operating unit delays the timing to resend the element by said delay value received from said main memory controller.

5 18. The method of controlling a memory according to claim 16, further comprising the step of:

if a deadlock state in which an overflow of said VSC address buffer and a resending of an element from said asynchronously operating unit are repeated is
10 detected, sending a delay value for shifting the timing to resend the element from said asynchronously operating unit from said main memory controller to said asynchronously operating unit;

wherein said asynchronously operating unit
15 delays the timing to resend the element by said delay value received from said main memory controller.